REMARKS/ARGUMENTS

Claims 1-20 are pending. No claim has been amended, canceled or added.

Claims 1 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tanaka in view of Park et al. Applicant respectfully traverses the rejection. The Examiner noted that Tanaka does not disclose "etching the first inter-layer insulation layer without exposing the first barrier layer," as recited in claim 1. The Examiner asserts Park et al. remedies the deficiency of Tanaka. Applicant disagrees. Contrary to the Examiner's assertion, Park et al. does not disclose or suggest the above recited feature.

Fig. 4D of the present application shows one implementation of the claimed invention. A first barrier layer 41 and a first inter-layer insulation layer 42 are "formed sequentially." See, e.g., step (b) of claim 1 and Fig. 4D. The first inter-layer insulation layer 42 is etched "without exposing the first barrier layer." See, e.g., step (c) of claim 1 and Fig. 4D. As a result, a partial portion 42A of the first inter-layer insulation layer 42 remains on over the first barrier layer 41. See, Fig. 4D.

The Examiner stated that Fig. 5B and column 6, lines 17 to 39 disclose the features, "etching the first inter-layer insulation layer without exposing the first barrier layer, so that at least a partial portion of the first inter-layer insulation layer remains over the first barrier layer between the bit line patterns" of claim 1. The Examiner appears to be asserting that an optional second nitride layer 112 shown in Fig. 5B of Park et al. corresponds to the partial portion 42A of the first inter-layer insulation layer 42 of the present invention. Applicant respectfully disagrees. The nitride layer 112 appears to be an etch stop layer that is used to etch the oxide layer 108. That is, the oxide layer is etched through until the nitride layer 112 is exposed, as shown in Fig. 5B of Park et al. Accordingly, the two layers 108 and 112 are of different materials - oxide and nitride. Note the nitride layer 112 is about 50 to 100 Å and is very thin (column 6, lines 24-28) since it is as an etch stop. Accordingly, the etching of the oxide layer 108 is continued until the nitride layer 112 is exposed. However, claim 1 recites "etching the first inter-layer insulation layer without exposing the first barrier layer" (emphasis added); i.e., a partial portion of the first inter-layer insulation layer remains over the first barrier

layer. Park et al., therefore, does not disclose the above recited features of claim 1 and thus does not remedy the deficiency of Tanaka. Claim 1 is allowable at least for this reason.

Among other features, claim 11 recites, "etching the first inter-layer insulation layer until a second space is defined between the first and second bit line patterns without exposing the first barrier layer provided between the first and second bit line patterns" (emphasis added). Neither Tanaka nor Park et al, alone or in combination, disclose or suggest these features. Claim 11 is allowable.

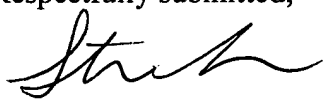
Claims 2-10 and 12-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tanaka and Park et al. in view of Huang. Applicants respectfully traverses the rejection. The above claims depend from claim 1 or 11 and are allowable at least for this reason.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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